

IP Name:	Design of the Delay-locked Loops and 1.25Gb/s Data Recovery
Grade:	Verification
Process:	0.35um 1P4M
Foundry:	TSMC
Features:	With Butterworth Characteristic Low-Jitter DLL
Release Notes:	Frequency 125 MHz Band Width 1.25 MHz Charge Pump Current 120uA VCDL gain 14ns/2.4v
Supply Voltage (Min)	3.0 V
Supply Voltage (Max)	3.6
Operating Frequency (Max)	140 MHz
Operating Frequency (Min)	100 MHz
Power Consumption	32 mW @125MHz 3.3v
Clock Jitter	3.853ps(rms)&32.8ps(PkPk)
Gate Count	1623
Die Size	2.25 mm2
Aspect Ratio	1

